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MANUFACTURE OF CHIP-TYPE ELECTRONIC COMPONENT

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Claim

Manufacture of semiconductor chips wherein

multiple top electrodes are formed on the top face of a mother board containing multiple boards, as well as formation of the bottom face multiple bottom electrodes conductive to each of the top electrodes;

multiple elements are mounted on the top face of the mother board and each element and each of the aforementioned top electrodes are electrically connected;

a sealing mother cap with multiple depressions formed on the bottom face is affixed onto the aforementioned mother board so as to seal each element in each depression; and

after this, the mother board and the sealing mother cap are cut apart for each element.

Detailed explanation of the invention

Industrial application field

The present invention pertains to a method for manufacturing chip-type electronic components. Specifically, for instance, it pertains to a method for manufacturing chip-type electronic components comprised by sealing elements such as ICs or elastic surface wave devices in a package.

Prior art

A compact seal type package used at present is a package (51) with leads such as illustrated in Figure 9. This is comprised by mounting an element on the top face of a board (53) to the bottom face of which multiple leads (52) are attached thus electrically conducting the element with the leads (52); and by covering a cap (54) on the board (53), the element is sealed in a package (55) comprised of the board (53) and the cap (54). Then, to package this electronic component onto a circuit board (56), the leads (52) are placed on top of electrodes (57) of the circuit board (56), and the leads (52) and the electrodes (57) are soldered (58) together.

On an electronic component with this structure, since soldering is relatively often used to connect leads and electrodes on the circuit board, there is a problem that variation in solder amount causes variation in the high frequency characteristics of the element. Further, since the positions at which the leads are attached to the board are not very precise, automatic packaging is difficult.

Japanese Kokai Patent Application No. Hei 2[1990]-87557 discloses a leadless package and its manufacturing method, wherein a surface electrode formed on the surface of a board is used as an electrode for external connection without using leads. Figure 10 illustrates a step of this manufacturing method. In this manufacturing method, on the top and the bottom faces of a mother

board (61) containing multiple boards, multiple top electrodes and bottom electrodes are respectively provided; each of the top and bottom electrodes is allowed to conduct by means of a through hole (62) on the mother board (61); multiple elements (63) are mounted on this mother board (61) and wire bonding is applied between top electrodes and elements (63); after that, as illustrated in Figure 10, a cap (64) is placed on top of each of the elements (63) one to one so as to seal each element (63) inside the cap (64); then the mother board (61) is cut for each element; thereby chip-type electronic components are manufactured.

The work of putting one cap each onto each of the elements and bonding each of the caps is troublesome in the manufacturing process; and the manufacturing efficiency is low.

Problem to be solved by the invention

The present invention was developed considering the aforementioned drawbacks of the prior art. The objective is, in the manufacture of electronic components, to improve the manufacturing efficiency by covering multiple elements with caps all at once.

Means to solve the problem

The manufacture of semiconductor chips according to the present invention is characterized in that multiple top electrodes are formed on the top face of a mother board containing multiple boards, as well as formation on the bottom face of multiple bottom electrodes conductive to each of the top electrodes; multiple elements are mounted on the top face of a mother board and each element and each of the aforementioned top electrodes are electrically connected; a sealing mother cap with multiple depressions formed on the bottom face is affixed onto the aforementioned mother board so as to seal each element in each depression; and after this, the mother board and the sealing mother cap are cut apart for each element.

Operation

In the present invention, after mounting multiple elements on top of a mother board that will be cut into multiple boards, a sealing mother cap having multiple depressions on the bottom face and that will be cut into multiple caps is placed on the board; thereby each element is sealed in each of the depressions. Therefore, multiple elements can be sealed all at once, and the work of putting each cap onto each of multiple elements one by one after mounting the elements on a mother board as in the prior art can be eliminated. As a result, the manufacturing efficiency of chip-type electronic components will improve further.

Application example

Next, an application example of the present invention will be explained in detail based on the attached figures.

A mother board (1) is formed by laminating multiple green sheets; and for instance, is manufactured as follows: first, the raw material is prepared by adding additives to ceramic powder such as SiO_2-BaO-Al_2O_3, which is calcinated and then ground, and mixed with a binder resin, plasticizer or the like after grinding. Then, a green sheet is formed by a doctor blade method or the like. Multiple green sheets are laminated, and the green sheets are pressed at a temperature of 50-100°C with an added pressure of 150-250 kgf, and thereby a pre-baked mother board (1) is obtained. Then, with a value controlled NC drill, NC punch, or the like, multiple piercing holes (2) are made through the mother board (1). After this, on the top face of the mother board (1), a conductive paste such as a Cu system paste is printed, and a top pattern electrode (3) such as illustrated in Figure 1(a) is formed. This top pattern electrode (3) has a pattern wherein multiple top electrodes (5) are placed continuously so that when the mother board (1) is cut into individual boards (4), each part will become a top electrode (5) (see Figure 6) of the board (4). In the same manner, conductive paste is printed on the bottom face of the mother board (1), and a ring-shaped bottom pattern electrode (6) such as is illustrated in Figure 1(b) is formed. This bottom pattern electrode (6) also has a pattern wherein multiple bottom electrodes (7) are placed continuously so that when the mother board (1) is cut, each part will become a bottom electrode (7) (see Figure 7) of the board (4). Furthermore, conductive paste is printed on the inner circumferential face of each piercing hole (2) of the mother board (1) so that a through hole (8) is formed. Naturally, the top pattern electrode (3) and the bottom pattern electrode (6) on the faces of the mother board (1) are electrically inter-conductive through the through hole (8). After this, both the mother board (1) and the conductive paste are concurrently baked in a non-oxidizing atmosphere at a temperature of 950-1000°C; and thereby the mother board (1) is completed. The example illustrated in Figure 1(a) and (b) is a mother board (1) yielding 9 boards. Finally, it is cut apart at the broken lines into individual boards (4).

The sealing mother cap (9) has dimensions that are about the same as those of the mother board (1); and on the bottom face, multiple depressions 10 are provided. The sealing mother cap (9) illustrated in Figure 2 (a) is also one that yields 9 caps. It is eventually cut apart at the broken lines, and a depression (10) is placed in the middle of the part that will be one cap surrounded by the broken lines. This sealing mother cap (9) is manufactured, as illustrated in Figure 2(b), by laminating and pressing a green sheet (12) with multiple piercing holes (11) made by punching or the like and a green sheet (13) without any holes, so as to form depressions (10) on the bottom face; and the laminated green sheets are then baked.

The mother board (1) manufactured as described above is fed to the packaging step of the elements (14) with the mother board (1) as the work size without cutting. First, Au-plating is applied to the top and bottom pattern electrodes (3) and (6) of the mother board (1) and the through holes (8). Then, as illustrated in Figure 3, in the middle locations between four through holes (8), all elements (14) are mounted; and by die-bonding, each element (14) and the top pattern electrode (3) are bonded with wires (15). Incidentally, an element (14) and top electrode may also be bump-connected using a bump provided on the bottom face of the element.

After this, as illustrated in Figure 4, from the top of elements (14) to the top of the mother board (1), the sealing mother cap (9) is placed, containing each element (14) in a depression (10). Using an adhesive or the like, the bottom face of the sealing mother cap (9) is bonded to the top face of the mother board (1), and an element (14) is sealed in each depression (10) air-tight. After completing the sealing, both the mother board (1) and the sealing mother cap (9) are cut with a dicing saw along the dashed line C-C as illustrated in Figure 4 (or the broken lines in Figures 1 and 2); thereby multiple chip-type electronic components (16) such as illustrated in Figure 5 will be obtained. That is, as illustrated in Figure 6, the mother board (1) will be separated into each of the boards (4); and at the same time, the sealing mother cap (9) will be separated into each of the caps (17). Thereby, an element (14) will be sealed in the package (18) comprised of the board (4) and the cap (17). Further, the top pattern electrodes (3) and the bottom pattern electrodes (8) will be respectively cut into the top electrodes (5) and the bottom electrodes (7) such as illustrated in Figures 6 and 7. Furthermore, a through hole (8) will be divided into four parts, and become side electrodes (19) formed at the corner parts of the board (4).

The chip-type electronic components (16) manufactured as described above are leadless. Without using leads, they will be directly connected with solder (22) to the electrodes (21) of a circuit board (20) as illustrated in Figure 8. Therefore, unlike a case using leads, occurrence of floating capacity at the junction part between the leads and the board can be prevented, as well as prevention of variation of wiring impedance depending on the length of the lead; and consequently, the high frequency characteristics can be good.

Further, since no leads are used and the component is made into a chip component, it can be taped and fed into an automatic packaging machine or the like, and thus it is also suitable for automatic packaging. Besides, this chip-type electronic component (16) has perpendicular edges (24) at four corners. In this manner, if perpendicular edges (24) are provided at two corners or more, rotation in the emboss can be prevented at the time of taping.

Further, as each cap (17) is installed onto each board (4) by cutting the sealing mother cap (9) affixed onto the mother board (1), the work of installing each cap (17) onto an element (14) one by one is eliminated; thus the manufacturing process will be simpler.

In the aforementioned application example, as a means to allow a top electrode and a bottom electrode to be conductive with each other, a through hole is used. However, other than this method, a top electrode and bottom electrode can be made conductive by means of a layer-built electrode or the like.

Effect of the invention

According to the present invention, the complicated work of putting a cap onto each element one by one after mounting elements on a mother board as required in the prior art can be eliminated; and instead, multiple elements can be sealed all at once. As a result of this, chip-type electronic components with small variation in high frequency characteristics and which are also suitable for automatic packaging can be manufactured more efficiently.

Brief description of the figures

Figure 1(a) and (b) and Figure 4 are explanatory diagrams illustrating the manufacture of an application example of the present invention. Figure 1(a) and (b) show a top view and a bottom view of a mother board. Figure 2 (a) and (b) show a bottom view and a partially broken enlarged cross-sectional view of the sealing mother cap. Figure 3 is a cross-sectional view illustrating a state wherein elements are mounted on the mother board. Figure 4 is a cross-sectional view illustrating a state wherein the elements are sealed in depressions by laminating the sealing mother cap. Figure 5 is an oblique view of a chip-type electronic component manufactured in the aforementioned method. Figure 6 is an exploded oblique view of the same chip-type electronic component. Figure 7 is a bottom view of the same chip-type electronic component. Figure 8 is an oblique view illustrating a state wherein the same chip-type electronic component is packaged on a circuit board. Figure 9 is a cross-sectional view illustrating a package with leads of the prior art and its packaging state. Figure 10 is a partially broken front view illustrating a step of the method for manufacturing a chip-type electronic component of another example in the prior art.

Explanation of symbols

1 Mother board
4 Board
5 Top electrode
7 Bottom electrode
9 Sealing mother cap
10 Depression
14 Element

//insert//

Figure 1

Key: 1 Mother board

Figure 2

Key: 9 Seating mother cap
10 Depression

Figure 3

Key: 14 Element

Figure 4

Figure 5

Key: 4 Board

Figure 6

Key: 5 Top electrode

Figure 7

Key: 7 Bottom electrode

Figure 8

Figure 9

Figure 10

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審査請求　未請求　請求項の数 1　(全5頁)

⑤4発明の名称　チップ型電子部品の製造方法

⑳特　願　平2−274359
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明　細　書

1．発明の名称

チップ型電子部品の製造方法

2．特許請求の範囲

(1)　複数個分の基板を含む親基板の上面に複数個分の上面電極を形成すると共に下面に各上面電極と導通した複数個分の下面電極を形成し、

親基板の上面に複数個の素子を搭載して各素子と前記各上面電極とを電気的に接続させ、

下面に複数個の凹所を形成された封止用親蓋を前記親基板の上に固着させて各素子を各凹所内に封入させ、

この後、親基板及び封止用親蓋を各素子毎に切り離すことを特徴とする半導体チップの製造方法。

3．発明の詳細な説明

[産業上の利用分野]

本発明はチップ型電子部品の製造方法に関する。具体的には、例えば、ＩＣや弾性表面波デバイス等の素子をパッケージ内に封入したチップ型電子部品の製造方法に関する。

[背景技術]

現在実用化されている小型の密閉型パッケージは、第９図に示すようなリード付きパッケージ５１である。これは、下面に複数本のリード５２を取着された基板５３の上面に素子を搭載して素子とリード５２とを電気的に導通させ、基板５３にキャップ５４を被せて基板５３とキャップ５４からなるパッケージ５５内に素子を封入したものである。しかして、この電子部品を回路基板５６に実装する場合には、回路基板５６の電極５７の上にリード５２を乗せ、リード５２と電極５７とをハンダ５８で半田付けしている。

しかしながら、このような構造の電子部品では、リードと回路基板上の電極とを接続する際にハンダを比較的多く使用するため、半田量のバラツキによって素子の高周波特性にバラツキを生じさせるという問題があった。また、リードの基板への取付位置精度が悪いため、自動実装も困難であった。

そこで、特開平２−８７５５７号公報には、リ

ードを無くして基板表面に形成した表面電極を外部接続用の電極としたリードレスパッケージ及びその製造方法が開示されている。第１０図は、この製造方法の１工程を示している。この製造方法は、複数個の基板を含む親基板６１の上面及び下面にそれぞれ複数の上面電極及び下面電極を設け、各上面及び下面電極を親基板６１のスルーホール６２によって導通させ、この親基板６１の上に複数個の素子６３を搭載して上面電極と素子６３との間にワイヤーボンディングを施した後、第１０図に示すように、各素子６３の上に１つ１つキャップ６４を被せて各素子６３をキャップ６４内に封入させ、ついで親基板６１を各素子毎にカットしてチップ型電子部品を製造していた。

このため、製造工程においてキャップを各素子の上に１つ１つ被せて接着してゆく作業が煩わしく、製造効率が悪かった。

［発明が解決しようとする課題］

本発明は、叙上の従来例の欠点に鑑みてなされたものであり、その目的とするところはチップ型電子部品の製造方法において、複数個の素子に一度にキャップを被せることができるようにし、その製造効率を向上させることにある。

［課題を解決するための手段］

本発明のチップ型電子部品の製造方法は、複数個分の基板を含む親基板の上面に複数個分の上面電極を形成すると共に下面に各上面電極と導通した複数個分の下面電極を形成し、親基板の上面に複数個の素子を搭載して各素子と前記各上面電極とを電気的に接続させ、下面に複数個の凹所を形成された封止用親蓋を前記親基板の上に固着させて各素子を各凹所内に封止させ、この後、親基板及び封止用親蓋を各素子毎に切り離すことを特徴としている。

［作用］

本発明にあっては、カットされて複数個の基板となる親基板の上に複数個の素子を搭載した後、下面に複数個の凹所を有しカットされて複数個のキャップとなる封止用親蓋を基板の上に被せて各凹所内に素子を封止させている。したがって、複数個の素子を一度に封止させることができ、従来例のように親基板の上に素子を搭載した後、複数個の素子に１つ１つキャップを被せるという繁雑な作業を無くすことができる。この結果、チップ型電子部品の製造効率がより一層向上する。

［実施例］

以下、本発明の実施例を添付図に基づいて詳述する。

親基板１は、複数枚のグリーンシートを積層して形成されており、例えば次のようにして製造される。まず、SiO_2-BaO-Al_2O_3等のセラミック粉末に添加物を加えて原料を調整し、これを仮焼した後に粉砕し、粉砕粉にバインダー樹脂や可塑剤等を混合する。つぎに、ドクターブレード法などによってグリーンシートを成形し、複数枚のグリーンシートを積層し、５０～１００℃の温度で１５０～２５０kgfの圧力を加えてグリーンシートを圧着させて未焼成の親基板１を得る。次に、数値制御のＮＣドリルやＮＣパンチなどによって親基板１に複数個の貫通孔２を穿孔する。この後、親基板１の上面にCu系ペースト等の導電ペーストを印刷し、第１図(a)に示すような上面パターン電極３を形成する。この上面パターン電極３は、親基板１を各基板４にカッティングした時、それぞれの部分が基板４の上面電極５（第６図参照）となるよう複数個の上面電極５が連続したパターンとなっている。同様に、親基板１の下面に導電ペーストを印刷し、第１図(b)に示すような環状の下面パターン電極６を形成する。この下面パターン電極６も、親基板１のカッティング時に、それぞれの部分が基板４の下面電極７（第７図参照）となるように複数個の下面電極７が連続したパターンとなっている。さらに、親基板１の貫通孔２の内周面には導電ペーストが印刷されてスルーホール８が形成される。もちろん、親基板１の両面の上面パターン電極３と下面パターン電極６とは、スルーホール８を介して互いに電気的に導通させられている。この後、親基板１と導電ペーストとを非酸化雰囲気において９５０～１０００℃の温度で同時に焼成することによって親基板１ができ

あがる。第１図(a)(b)に示してあるものは、９個取りの親基板１であり、最終的には破線の箇所で個々の基板４に切り離されるものである。

また、封止用親蓋９は、親基板１とほぼ同じ寸法を有しており、その下面には複数個の凹所１０が設けられている。第２図(a)に示す封止用親蓋９も、９個取りであり、最終的には破線の箇所で切り離されるものであり、凹所１０は破線で囲まれた１つのキャップとなる部分の中央に配置されている。この封止用親蓋９は、第２図(b)に示すように、パンチング等によって複数個の通孔１１を穿孔されたグリーンシート１２と孔のないグリーンシート１３とを積層及び圧着させて下面に凹所１０を形成し、これを焼成して製作される。

上記のようにして製造された親基板１は、切り離されることなく、親基板１をワークサイズとして素子１４の実装工程へ送られる。まず、親基板１の上面及び下面パターン電極３，６及びスルーホール８には、Auメッキが施され、ついで第３図に示すように、四つのスルーホール８の中間位置に各々素子１４が搭載されてダイボンディングされ、各々の素子１４と上面パターン電極３の間がワイヤー１５によりボンディングされる。なお、素子１４と上面電極とは、素子の下面に設けたバンプを用いてバンプ接続してもよい。

この後、第４図に示すように、素子１４の上から親基板１の上に封止用親蓋９を被せて各素子１４を凹所１０内に納め、接着剤等を用いて封止用親蓋９の下面を親基板１の上面に接着し、素子１４を各凹所１０内に気密的に封入する。封止が完了した後、親基板１及び封止用基板９を第４図の一点鎖線Ｃ－Ｃ（もしくは、第１図及び第２図の破線）に沿ってダイシングソーでカットすることにより、第５図に示すようなチップ型電子部品１６が複数個得られる。すなわち、第６図に示すように、親基板１は各基板４に分離され、同時に封止用親蓋９は各キャップ１７に分離され、素子１４は基板４とキャップ１７からなるパッケージ１８内に封止される。また、上面パターン電極３及び下面パターン電極８は、それぞれカットされて第６図及び第７図に示すような上面電極５と下面電極７になる。さらに、スルーホール８は４つに分割され、基板４のコーナ部に形成された側面電極１９となる。

上記のようにして製造されたチップ型電子部品１６はリードレスタイプであり、リードを用いることなく、第８図に示すように回路基板２０の電極２１にハンダ2-2で直接に接合されるものである。従って、リードを用いた場合のようにリードと基板との接合部分に浮遊容量が発生したり、リードの長さによって配線インピーダンスが大きくなったりすることを防止でき、高周波特性を良好にすることができる。

また、リードがなく；チップ部品化されているので、テーピングして自動実装機などに供給することができ、自動実装にも適している。しかも、このチップ型電子部品１６は、４箇所に直角になったエッジ２４を有している。このように少なくとも２箇所以上に直角になったエッジ２４を有していれば、テーピングの際にエンボス内での回転を防止することができる。

また、親基板１の上に固着させた封止用親蓋９をカットすることによって各キャップ１７を各基板４の上に取り付けているので、１つ１つキャップ１７を素子１４の上に取り付けてゆく作業がなくなり、製造工程が簡単になる。

なお、上記実施例では、上面電極と下面電極とを導通させる手段としてスルーホールを用いているが、これ以外にも積層電極等によって上面電極と下面電極を導通させるようにしてもよい。

[発明の効果]

本発明によれば、従来例のように親基板の上に素子を搭載した後、各素子に１つ１つキャップを被せるという繁雑な作業を無くすことができ、複数個の素子を一度に封止させることができる。この結果、高周波特性のバラツキが小さく、自動実装にも好適なチップ型電子部品をより効率的に製造することができる。

４．図面の簡単な説明

第１図(a)(b)ないし第４図は本発明の一実施例

の製造方法を示す説明図であって、第１図(a)(b)は親基板の上面図及び下面図、第２図(a)(b)は封止用親蓋の下面図及び一部破断した拡大断面図、第３図は親基板の上に素子を搭載した状態を示す断面図、第４図は親基板の上に封止用親蓋を積層して凹所内に素子を封止した状態を示す断面図である。第５図は同上の方法によって製造されたチップ型電子部品の斜視図、第６図は同上のチップ型電子部品の分解斜視図、第７図は同上のチップ型電子部品の下面図、第８図は同上のチップ型電子部品を回路基板に実装した状態を示す斜視図である。第９図は従来例のリード付きパッケージとその実装状態を示す断面図、第１０図は別な従来例のチップ型電子部品の製造方法の一工程を示す一部破断した正面図である。

１…親基板
４…基板
５…上面電極
７…下面電極
９…封止用親蓋
１０…凹所
１４…素子

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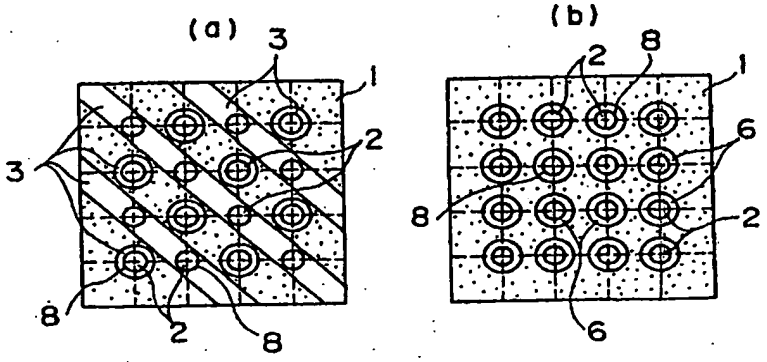
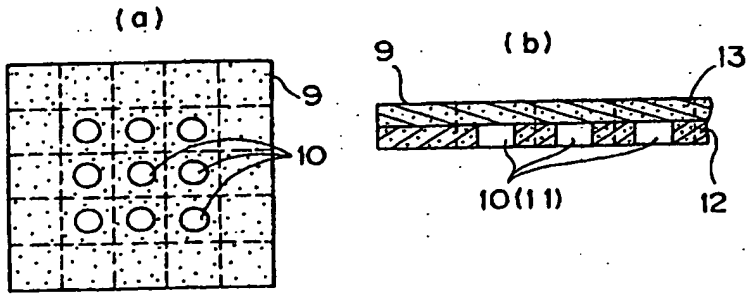
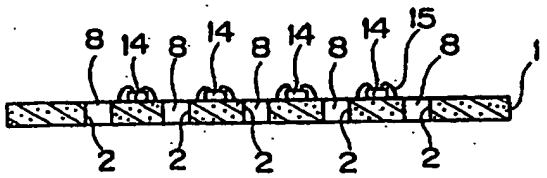
第１図



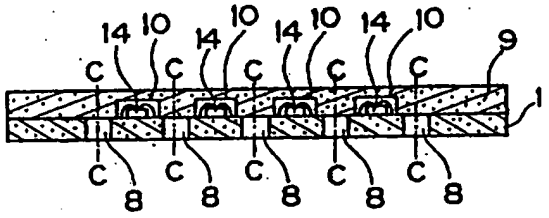
第２図



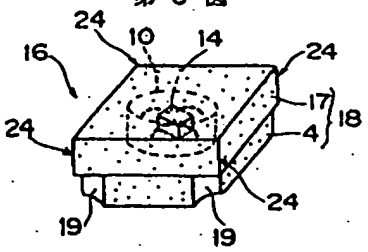
第3図　14…素子



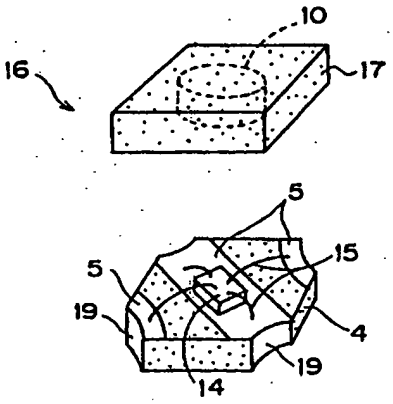
第4図



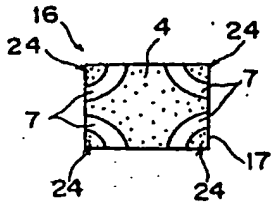
第5図　4…基板



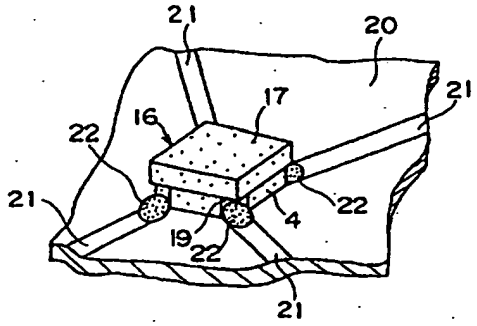
第6図　5…上面電極



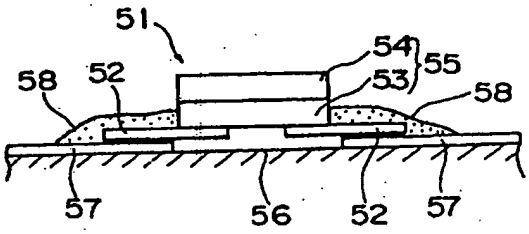
第7図　7…下面電極



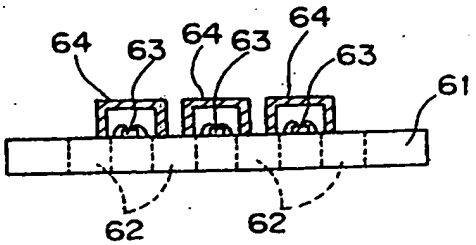
第8図



第9図



第10図



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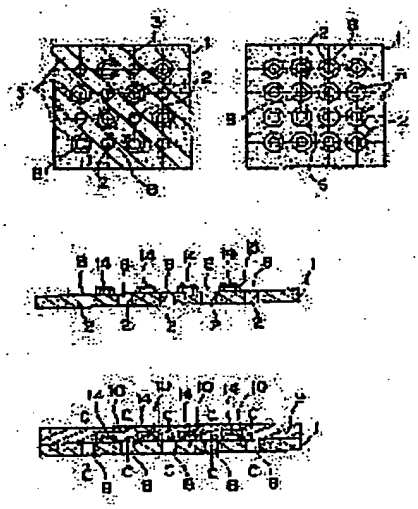
(54) MANUFACTURE OF CHIP TYPE ELECTRONIC COMPONENT

(57)Abstract:
PURPOSE: To enable a plurality of devices to be capped at a time by mounting a plurality of devices on a mother board which is to be cut into a plurality of boards and then by covering the board with a sealing mother cap which has a plurality of recesses in the bottom and is to be cut into a plurality of caps to seal devices in the respective recess.
CONSTITUTION: Top and bottom pattern electrodes 3, 6 and through holes 8 of a mother board 1 are Au-plated, where each device 14 is mounted at the medium position of four through holes 8 and bonded: this device 14 is bonded to a top pattern electrode 3 with wires 15. Thereafter, devices 14 are placed in the respective recesses 10 by covering the the mother board 1 from above the devices 14 with a sealing mother cap 9, thereby hermetically encapsulating the devices 14 in the recesses 10. After sealing is completed, the mother board 1 and the sealing mother cap 9 are cut by a dicing saw into a plurality of chip-type electronic components.



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